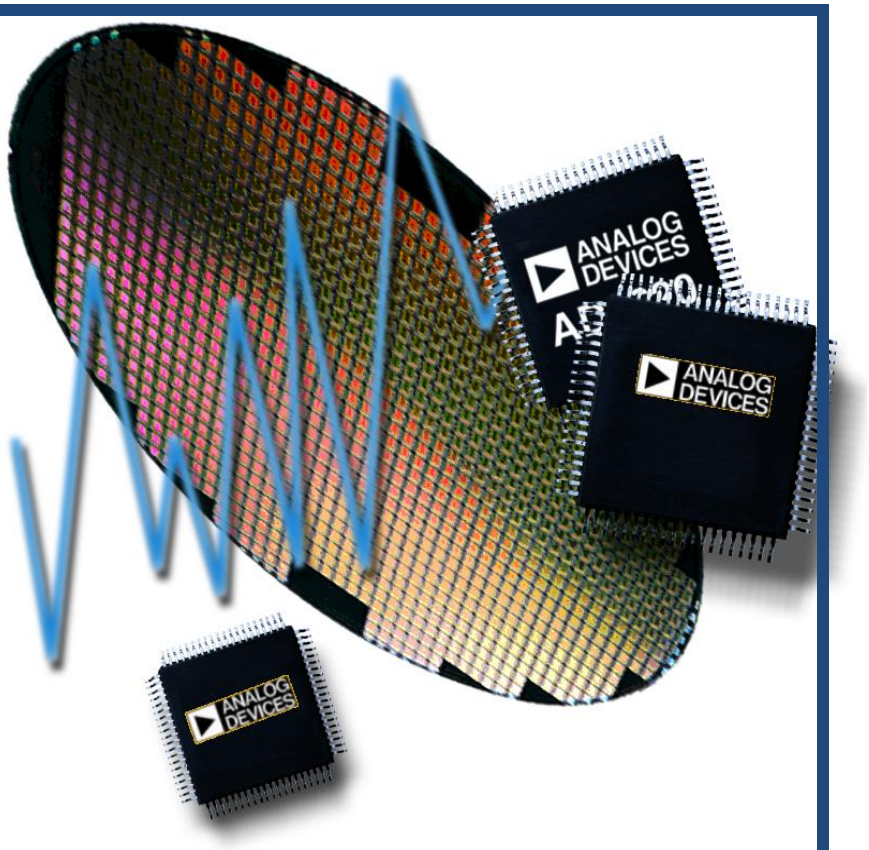

Reliability Report

Report Title: 2x2 LFCSP at JC2 Qualification

Report Number: 19661

Revision: A

Date: 18 July 2022

Summary

This report documents the successful completion of the reliability qualification requirements for the release of the 2x2 LFCSP package assembled at JC2. The ADP123 is the device vehicle used for this qualification. The ADP123 is a low quiescent current, low dropout linear regulator. It is designed to operate from an input voltage between 2.3 V and 5.5 V and to provide up to 300 mA of output current. The low 85 mV dropout voltage at a 300 mA load improves efficiency and allows operation over a wide input voltage range. Table 1 describes the ADP123 product characteristics.

Table 1: ADP123 Product Characteristics

Die/Fab

Die Id	TMAC80 A
Die Size (mm)	0.99 x 1.15
Wafer Fabrication Site	E_TSMC0308
Wafer Fabrication Process	0.35um CMOS
Approximate Transistor Count	3,130
Passivation Layer	undoped-oxide/OxyNitride
Bond Pad Metal Composition	AlCu(0.5%)

Package/Assembly

Package	6-LFCSP
Body Size (mm)	2.00 x 2.00 x 0.55
Assembly Location	JCET (JC2)
Molding Compound	Hitachi CEL 9240HF10
Die Attach	Hitachi EN 4900GC conductive
Wire Type	4N Gold
Wire Diameter (mils)	1.0
Lead Frame Material	Copper
Lead Finish	NiPdAu
Moisture Sensitivity Level	1
Maximum Peak Reflow Temperature (°C)	260

Description / Results of Tests Performed

Table 2 provides a description of the qualification tests conducted and the associated test results for products manufactured on the same technologies as described in Table 1. All devices were electrically tested before and after each stress. Any device that did not meet all electrical data sheet limits following stressing would be considered a valid (stress-attributable) failure unless there was conclusive evidence to indicate otherwise.

Table 2: LFCSP at JCET (JC2) Package Qualification Test Results

Test Name	Specification	Conditions	Device	Lot #	Sample Size	Qty. Failures
High Temperature Storage Life (HTSL)	JESD22-A103	150°C, 1,000 Hours	ADP123	Q19661.1.HS1	77	0
Solder Heat Resistance (SHR) [1]	J-STD-020	MSL-1	ADP123	Q19661.1.SH1	11	0
				Q19661.2.SH2	11	0
				Q19661.3.SH3	11	0
Temperature Cycling (TC) [1]	JESD22-A104	-65°C/+150°C, 500 Cycles	ADP123	Q19661.1.TC1	77	0
				Q19661.2.TC2	77	0
				Q19661.3.TC3	77	0
Unbiased HAST (UHST) [1]	JESD22-A118	130C 85%RH 33.3 psia, 96 Hours	ADP123	Q19661.1.UH1	77	0
				Q19661.2.UH2	77	0
				Q19661.3.UH3	77	0

[1] These samples were subjected to preconditioning (per J-STD-020 Level 1) prior to the start of the stress test. Level 1 preconditioning consists of the following: Bake: 24 hrs @ 125°C, Unbiased Soak: 168 hrs @ 85°C, 85%RH, Reflow: 3 passes through an oven with a peak temperature of 260°C.

Samples of the many devices manufactured with these package and process technologies are continuously undergoing reliability evaluation as part of the ADI Reliability Monitor Program. Additional qualification data is available on Analog Devices' web site.

ESD Test Results

The results of Field-Induced Charged Device Model (FICDM) ESD testing is summarized in Table 3. ADI measures ESD results using stringent test procedures based on the specifications listed. Any comparison with another supplier's results should ensure that the same ESD test procedures have been used. For further details, please see the EOS/ESD chapter of the ADI Reliability Handbook (available via the 'Quality and Reliability' link on Analog Devices' web site).

Table 3: ADP123 ESD Test Results

ESD Model	Package	ESD Test Spec	RC Network	Highest Pass Level	First Fail Level	Class
FICDM	6-LFCSP	JS-002	1Ω, Cpkg	±1000V	±1250V	C3

Approvals

Reliability Engineer: Pernell Marc Mosuela

Additional Information

Data sheets and other additional information are available on Analog Devices' web site